power source, so that a drive discharge voltage is applied between said electrodes .

27. (AS NEW HEREIN) A plasma display panel device having first and second electrodes, spaced apart from one another, a third electrode arranged perpendicularly to said first and second electrodes, and a ground power source, and performing a display by generating a discharge between said first and second electrodes, said plasma display panel device comprising:

a drive circuit that, when a drive voltage pulse is to be applied between said first and second electrodes, applies the drive voltage pulse between said first and second electrodes, while maintaining the third electrode at a voltage potential of said ground power source, the voltage potential of said ground power source being between voltage potentials of said first electrode and said second electrode.

REMARKS

In accordance with the foregoing, amendments have been made to various of the independent claims for purposes of clarification and/or to avoid any possible confusion with somewhat similar recitations in related claims.

Particularly, claims 1 and 24 have been amended to change "a first drive voltage" and "a second drive voltage into, respectively, --a drive voltage-- and --another drive voltage--. This is to avoid any possible confusion with "first" and "second" recitations in claim 3 and subsequent claims.

Claims 3, 7 and 26 are amended to clarify the conditions of the "first state" and "second state" and, further, to clarify that in the "second state" the first or second electrode is connected to a second (claims 3 and 26) or third (claim 7) power source. See also similar amendments in claim 22.

Finally, a new claim 27 is presented which addresses the feature that when a discharge voltage pulse is applied between the first and second electrodes, the third electrode (address electrode) is maintained at the voltage of the ground power source. In this situation, the voltage of the ground power source is between the voltages of the first and second electrodes. This relates to the current claim 20 and the embodiment in the second paragraph of page 15. As shown in Fig. 4, when the sustain discharge pulse is applied between the first and second electrodes without connecting these electrodes to the ground power source, the address

electrode is maintained at the ground potential so as to avoid a storage, or a collision, of positive charges at the address electrode.

No new matter is presented and, accordingly, approval and entry of the foregoing amended and new claims are respectfully requested.

STATUS OF CLAIMS

All of the pending claims 1, 3-14, 16-24, and 26 are rejected.

ITEM 2: REJECTION OF CLAIMS 1 AND 3-26 FOR ANTICIPATION BY ANDOH (USP 4,044,349) UNDER 35 USC § 102(b)

ITEM 3: REJECTION OF THOSE SAME CLAIMS 1 AND 3-26 FOR ANTICIPATION UNDER 35 USC § 102(b) BY SAKUMA (USP 4,384,287)

The respective grounds for the rejections of items 2 and 3 are almost identical in content, differing only by the identity of the references (i.e., Andoh in Item 2 versus Sakuma in Item 3) and the portions of those references cited in support.

The present grounds, moreover, repeat the "original" grounds set forth in the Action of May 28, 2002 but, in each instance, the repeated content of the "original grounds" is interspersed with additional text corresponding to the amendments to the claims in the intervening Preliminary Amendment.

Generally, in each of items 2 and 3, the first portion of the grounds, extending to the citations of figures and of columns and lines, corresponds to claim 1; the second portion, in the last six lines of each of items 2 and 3 ("Andoh also discloses..." and "Sakuma also discloses..."), is somewhat of a combination of alternately interspersed recitations of independent claims 3 and 9 and possibly other independent claims, such as claims 22 and 24.

Applicants respectfully submit that the presentation of what appears to be a mixture of claim excerpts, extracted from various different, unidentified claims, purporting to read same on the disclosures of the references, is inaccurate and incapable of supporting the rejections of items 2 and 3.

COMPUTER SEARCH OF ANDOH USP '349 AND SAKUMA US '287 TERMS FOR THE REJECTED CLAIMS

A computer search of each of Andoh and Sakuma was conducted for the following terms of the claims:

ground

reference

power

source

supply

voltage supply

None of these terms was found in Andoh.

In Sakuma, "power" and "power supply" were found, but the term "power source" was not found nor is any of the other above terms.

The absence in the references of the above terms, as established by the computer search, refutes the Examiner's purported "readings" of the claims on the two references. Moreover, no explanation is provided for the Examiner's revisions to the prior grounds of rejection--e.g., as to how and why these revised "grounds" nevertheless are supported by the identical portions of the disclosure, of Andoh, i.e., Fig. 4 and col. 5, line 53 to col. 6, line 46 and of Sakuma, i.e., Figs. 6-12 and col. 5, lines 14-45 and col. 7, line 11-cool. 8, line 20 as in the prior Office Action.

Moreover, applicants explained in the Preliminary Amendment the fact that Andoh et al. and Sakuma fail to disclose the claimed features of this invention, much less render the same obvious or anticipated. The arguments of the Preliminary Amendment are incorporated herein by reference and are supplemented by the following.

ANDOH CLEARLY TEACHES USE OF A GROUND LEVEL (0 VOLTAGE) REFERENCE VOLTAGE

The Examiner's errors in contending that Andoh does not use a ground level reference voltage are readily revealed in the Examiner's expanded "Response to Arguments" in item 4 of

the present Action. Specifically, the Examiner asserts at page 4 of the Action:

> In Andoh Figs. 3, 4A, 4B, the `+$V_{w/2}$' and `-$V_{w/2}$' are merely reference sign [sic., -s] indicating the driving voltages are above and below the reference voltage `V_{xw}' by the same amount and not at ground level as erroneously alleged by applicant.

(Emphasis added)

The Examiner's argument is clearly misplaced. The designation V_{xw} is not a reference voltage but, instead, is the "name" of, or "label" put on, the write signal output from the X address driver 110 in Fig. 1 and shown in Fig. 4A. This same is true as to "V_{yw}" output by the Y address driver 111 in Fig. 1 and shown in Fig. 4B. The same is also true as to the X sustain signal V_{xs} shown in Fig. 4C and output from the sustain driver 112 in Fig. 1 and the Y sustain signal V_{ys} shown in Fig. 4D and likewise output from the sustain driver 112 in Fig. 1.

The fact that each of these signals V_{XW}, V_{yw}, V_{xs} and V_{ys} is merely the "name" of a driver signal and is not a voltage level is abundantly clear from the fact that none thereof is shown in Fig. 3. Instead, Fig. 3 illustrates voltage levels, relative to a "0" voltage reference level, of pulses which are contained in those signals. (See, e.g., col. 3, lines 42-47 and col. 6, lines 26-32)

Col. 5, line 60-col. 6, line 46 of Andoh--on which the Action relies in item 2, but incorrectly so--explains that the X and Y address drivers 110 and 111, respectively, alternately apply pulse voltages of $\pm 1/2V_W$ on the respective X and Y address electrodes, which combine to produce a voltage V_W higher than the firing voltage V_f and both of which, along with all other reference, or power supply, voltages levels are referenced to 0 volts in Fig. 3.

Moreover, the sustain driver 112 is shown to have switching transistors connected at series nodes in alternate pairs of a first set between $\pm 1/2V_{sa}$ voltage power terminals and of a second set between $\pm 1/2$ V_s voltage power terminals--and from which nodes the respective sustain voltages V_{xs} of Fig. 4C and V_{YS} of Fig. 4D are output in the respective T_W and T_d time intervals. In more detail, for V_{xs}, a first series node connects switching transistors Q_{X1} and Q_{X2}, which operate during the write interval T_W and a second series node connects switching transistors Q_{X3} and Q_{X4}, which operate during the display interval T_d and which respectively output the T_W and T_d intervals of the drive signal waveform V_{XS} of Fig. 4C.

Since the voltages V_W and V_S are shown relative to a 0 voltage reference level in Fig. 3, necessarily, in the sustain driver 112, the series interconnection nodes--between the transistor

pairs and to which the output signal lines, on which V_{XS} and V_{YS} are output--are likewise referenced to 0 voltage. This inescapably requires that the X and Y address drivers 110 and 111 likewise output the write voltages V_{XW} and V_{YW}, respectively of Figs. 4A and 4B, referenced to a 0 volt level.

SAKUMA LIKEWISE TEACHES A GROUND LEVEL (0 VOLTAGE) REFERENCE VOLTAGE

The Examiner's contentions to the contrary, as to Sakuma, are seen even more easily to be in error.

Fig. 3 illustrates that the source of transistor 6 is connected to ground (see col. 4, line 2), which establishes a 0 voltage reference for the input signal V_{in} applied to input terminal 2 in Fig. 3--and that input signal V_{in}, indeed, is shown in Fig. 4A to have a "0" voltage reference level. The power supply voltage V_0 at terminal 1 in Fig. 3 necessarily is referenced to the ground level at the source terminal of transistor 6 and is consistent with the 0 voltage, or ground, reference level of the signal V_0 in Fig. 4C (see also col. 4, line 32, explaining that Fig. 4C shows an output pulse train of high voltage V_0 at terminal 3 in Fig. 3).

The Examiner relies, more particularly, on Figs. 6 through 12 and col. 5, lines 14-45 through col. 7, line 7 to col. 8, line 20--but that reliance is likewise in error.

Fig. 6 is discussed at col. 5, line 14 et seq. as illustrating a "balanced-type drive method" in which high voltage output pulses of 150 volts and opposite phase are produced for supply to the column driver circuit 310 and the line driver circuit 320 by the respective switching circuits shown in Fig. 6 (col. 5, lines 30-37). In each of those switching circuits, the power voltage V_0 is set to 150 volts by the switching transistors 6 and 7 to produce output pulses switching between ground and V_0=150 volts, in out of phase relationship, on the output lines 31 and 32 as shown in Fig. 6--and which output pulses are shown in Figs. 7C and 7D, respectively. The opposite-phased pulse waveforms of Figs. 7C and 7D, each referenced to 0 volts, when added together produce the waveform of Fig. 7E--but in which the individual pulse waveforms of Figs. 7C and 7D both return to 0, or ground, volts.

The same analysis is applicable to the embodiments of Figs. 9 through 12C.

CONCLUSION

As argued in the Remarks of the Preliminary Amendment, the Andoh drive circuit uses voltages formulated on the same basis as shown in the prior art Figs. 24A and 24B in the present application -- i.e., the x drive signal voltage rises from ground "0" to +Vwx for the write pulse WP and the y drive signal voltage likewise rises from ground ("0") to +Vey for the pulse EP -- and, in both instances, the pulse, at its trailing edge, returns to ground.

With more particular reference to Figs. 4C and 4D, Vxs and Vys represent pulse wave forms applied to the X and Y electrodes, respectively, of each pair. In Vxs, the positive pulse of +Vsa/2 and the negative pulse of -Vsa/2 are applied within Tw and another positive pulse +Vs/2 and another negative pulse of -Vs/2 are applied within Td. Vsa and Vs are referenced to ground level ("0 volts") according to Fig. 3. Thus, the pulse wave Vxs during Tw, starts from the ground level and changes (i.e., rises or falls, respectively) to +Vxa/2 or -Vsa/2, and then returns to the ground level. Likewise, during Td, the pulse wave Vxs starts from the ground level and changes (i.e., rises or falls, respectively) to +Vs/2 or -Vs/2, and returns to ground level. Vys has the same wave form.

As long as the pulse wave starts at the ground level or returns to the ground level as in Andoh, there is a noise on the ground level which causes a level change in the ground level. According to the wave form of Vxs and Vys, the pulse wave returns to the ground level. Therefore, the noise is generated on the ground level.

According to the present invention and as recited generically in at least claim 1 -- and, variously, generically or more specifically in each of the independent claims -- the drive circuit employs power sources different from ground level so as to apply a first drive voltage when applying the drive voltage pulse, and employs power sources different from ground level so as to apply a second drive voltage when completing the drive voltage pulse. These "power sources" may be different from each other or the same, as shown in the various different embodiments. At the front edge of the drive voltage pulse, the sustain plasma discharge occurs between the first and second electrodes, and, at the back edge of the drive voltage pulse, the capacitor charge/discharge occurs between the electrodes. Therefore, at both of the front and the back edges, the voltage of the first and second electrodes is different from the ground level.

By contrast, in Andoh, at the back edge of the pulse, the voltage of the first and second electrodes is the ground level. Andoh thus is a "teaching-away" from the present, claimed

invention, and the deficiencies thereof are not overcome by Sakuma nor has *prima facie* obviousness of the combination been demonstrated.

By contrast, as shown in Fig. 4A of the application, the voltage swing of each of the X and the Y waveforms is between -V1 and +V2, passing through "0v." in that rise and, as well, passing through "0v." in the fall from +V2 to -V1. Thus, the rise does not begin from ground nor does the fall end at ground.

It is inescapably apparent that the circuitry of each of Andoh and of Sakuma suffer from the very same deficiency of the acknowledged prior art, as set forth in the related art discussion of the subject application--and which is overcome by the circuitry and method of the invention, as claimed.

REQUEST FOR INTERVIEW

Applicants repeat the request for interview which was discussed with the Examiner in the Fall of 2002, before the Examiner's departure on leave. It was understood the Examiner, upon her return at the end of November 2002, would entertain an interview before issuing a further Office Action. Hence, applicants were surprised to receive the December 2, 2002 Office Action.

Applicants attach hereto copies of Figs. 4A-7B of the application, which have been annotated to show current paths in Figs. 4B and 5B, corresponding to those shown in Figs. 6B and 7B in the drawings of the application, as filed, and which it is believed will assist the Examiner in better understanding the invention herein, as claimed (collectively designated as Exhibit A).

Further, submitted herewith as Exhibit B are two sheets of four separate waveforms relating, as labeled, respectively to claims 1, 22, and 24, claim 3, claim 5, and claims 7 and 9, illustrating "starting" and "completing" voltage levels of those waveforms--graphically illustrating the circumstance that they neither start nor stop (or "complete") at ground level, in accordance with the invention as claimed herein--and altogether distinguishing same from the waveforms of the references.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: April 2, 2003

By: _____
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CERTIFICATE UNDER 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231

on April 2, 2003

STAAS & HALSEY

By: _____

Date: 4-2-03

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please AMEND the following claims:

1. (THRICE AMENDED) A plasma display panel device having first and second electrodes, spaced apart from one another, and a ground power source and performing a display by generating a discharge between said first and second electrodes, said plasma display panel device comprising:

a drive circuit applying a drive voltage pulse between said first and second electrodes; wherein

when the drive voltage pulse is to be applied between said first and second electrodes, said drive circuit connects said first and second electrodes to power sources that are different from said ground power source so as to apply a [first] drive voltage between said first and second electrodes, and

when completing said drive voltage pulse, said drive circuit connects said first and second electrodes to power sources that are different from said ground power source so as to apply [a second] another drive voltage between the first and second electrodes.

3. (THRICE AMENDED) A plasma display panel device having first and second electrodes, spaced apart from one another, and a ground power source and performing a display by generating a discharge between said first and second electrodes, said plasma display panel device comprising:

a drive circuit that, when a drive voltage pulse is to be applied between said first and second electrodes, changes said first and second electrodes from a first state [of being] in which the first and second electrodes are connected to a first power source, different from said ground power source, to a second state [of being] in which the first or second electrode is connected to a second power source, different from said ground power source, so as to apply a drive voltage between said first and second electrodes [when a drive voltage pulse is to be applied between said first and second electrodes].

4. (AS TWICE AMENDED) The plasma display panel device according to claim 3, wherein:

said drive circuit returns said first and second electrodes to the first state, of being

connected to said first power source, upon completion of the application of said drive voltage pulse.

5. (AS TWICE AMENDED) A plasma display panel device having first and second electrodes, spaced apart from one another, and a ground power source and performing a display by generating a discharge between said first and second electrodes, said plasma display panel device comprising:

a drive circuit that changes said first and second electrodes from a first state of being connected to a first power source, different from said ground power source, to a second state of being respectively connected to second and third power sources, different from said ground power source, so as to apply a drive voltage between the two electrodes when a drive voltage pulse is to be applied between said first and second electrodes.

6. (AS TWICE AMENDED) The plasma display panel device according to claim 5, wherein:

said drive circuit returns said first and second electrodes to the first state, of being connected to said first power source, upon completion of the application of said drive voltage pulse.

7. (THRICE AMENDED) A plasma display panel device having first and second electrodes, spaced apart from one another, and a ground power source and performing a display by generating a discharge between said first and second electrodes, said plasma display panel device comprising:

a drive circuit that, when a drive voltage pulse is to be applied between said first and second electrodes, changes said first and second electrodes from a first state [of being] in which the first and second electrodes are respectively connected to first and second power sources, different from said ground power source, to a second state [of being] in which the first or second electrode is connected to a third power source, different from said ground power source, so as to apply a drive voltage between the two electrodes [when a drive voltage pulse is to be applied between said first and second electrodes].

8. (THRICE AMENDED) The plasma display panel device according to claim 7, wherein:

said drive circuit returns said first and second electrodes to the first state, of being connected to said first or second power source, upon completion of the application of said drive voltage pulse[s].

9. (AS TWICE AMENDED) A plasma display panel device having first and second electrodes, spaced apart from one another, and a ground power source and performing a display by generating a discharge between said first and second electrodes, said plasma display panel device comprising:

a drive circuit that changes said first and second electrodes from a first state of being respectively connected to first and second power sources, different from said ground power source, to a second state of being respectively connected to third and fourth power sources, different from said ground power source, so as to apply a drive voltage between the two electrodes when a drive voltage pulse is to be applied between said first and second electrodes.

10. (AS TWICE AMENDED) The plasma display panel device according to claim 9, wherein:

said drive circuit returns said first and second electrodes to the first state, of being respectively connected to said first and second power sources, upon completion of the application of said discharge voltage pulse.

11. (AS ONCE AMENDED) The plasma display panel device according to claim 5, wherein:

reversed-polarity discharge voltage pulses are applied to said first and second electrodes.

12. (AS ONCE AMENDED) The plasma display panel device according to claim 7, wherein:

reversed-polarity discharge voltage pulses are applied to said first and second electrodes.

13. (AS ONCE AMENDED) The plasma display panel device according to claim 9, wherein: